EXHIBIT 3

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Paper 9
Entered: June 23, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner,

v.

SOLAS OLED LTD.,
Patent Owner.

IPR2020-00320
Patent 7,446,338 B2

Before SALLY C. MEDLEY, JESSICA C. KAISER, and JULIA HEANEY, *Administrative Patent Judges.*

KAISER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314; 37 C.F.R. § 42.4

On December 18, 2019, LG Display Co. Ltd. ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1–3 and 5–13 of U.S. Patent No. 7,446,338 B2, issued on November 4, 2008 (Ex. 1001, "the '338 patent"). Paper 1 ("Pet."). Solas OLED Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). On April 27, 2020, we authorized additional briefing addressing a district court claim construction order. On May 4, 2020, Petitioner filed a Supplemental Pre-Institution Brief addressing the district court claim construction. Paper 7 ("Supplemental Brief" or "Supp. Br."). On May 11, 2020, Patent Owner filed a Response to Petitioner's Supplemental Pre-Institution Brief. Paper 8 ("Supplemental Response Brief" or "Supp. Resp. Br.").[1] Applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we grant Petitioner's request and institute an *inter partes* review of claims 1–3 and 5–13.

I. BACKGROUND

A. The '338 Patent (Ex. 1001)

The '338 patent describes a display panel comprised of pixels, the pixels having a particular arrangement of transistors driving the pixels' light-emitting elements. Ex. 1001, 2:34–41, code (57). Figure 1 of the '338 patent is reproduced below.

[1] Additionally, on May 14, 2020, we denied Patent Owner's May 12, 2020 request for supplemental briefing to address *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB March 20, 2020) (precedential). Ex. 3001. Specifically, we denied Patent Owner's request because Patent Owner's Preliminary Response did not request that the Board exercise its discretion under 35 U.S.C. § 314(a) or address *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (Sept. 12, 2018) (precedential).

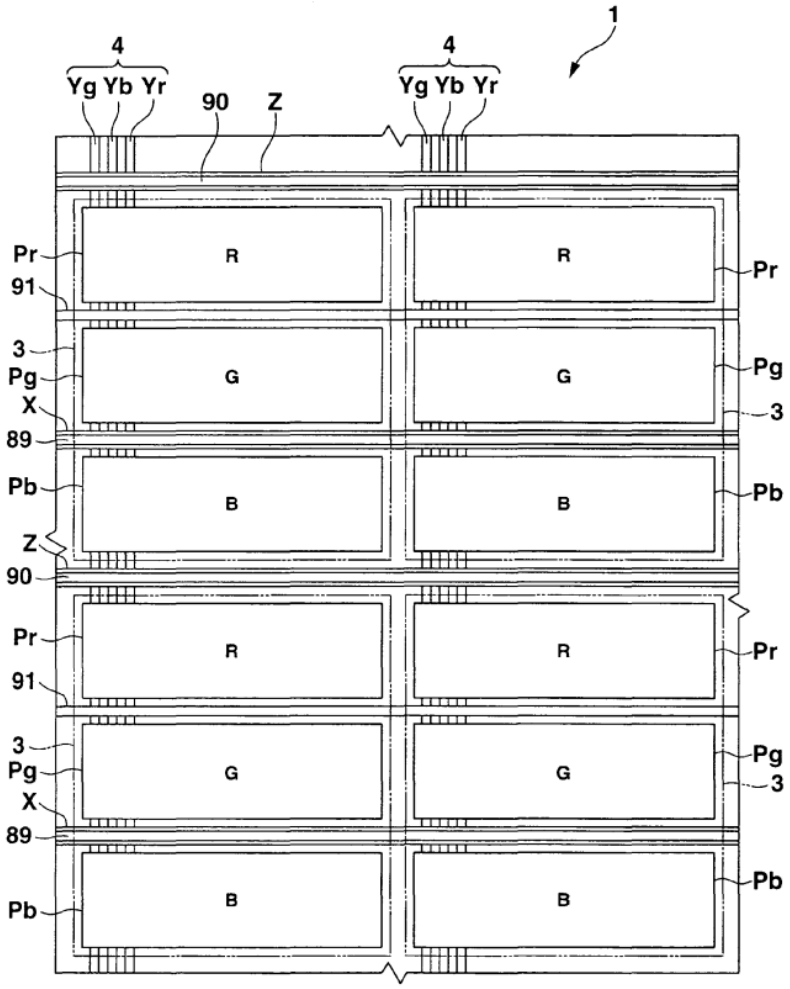


FIG.1

Figure 1 shows four adjacent pixels in display panel 1. Display panel 1 is comprised of pixels 3; in particular, the figure shows four adjacent pixels arranged in a 2-by-2 configuration, i.e., the pixels are arranged in an array. *Id.* at 4:53–55, 4:65–66. Each pixel 3 is comprised of red sub-pixel Pr, green sub-pixel Pg, and blue sub-pixel Pb. *Id.* at 4:63–65. Each sub-pixel Pr, Pg, Pb is connected to corresponding signal line Yr, Yb, Yg, respectively. *Id.* at 5:12–15. Further, each sub-pixel is connected to select interconnection 89, feed interconnection 90, and common interconnection

91. *Id.* at 5:23–40; *see id.* at 6:47–48. Still further, each sub-pixel Pr, Pg, Pb have a similar circuit arrangement. *Id.* at 6:47–48.

Figure 2 is reproduced below.

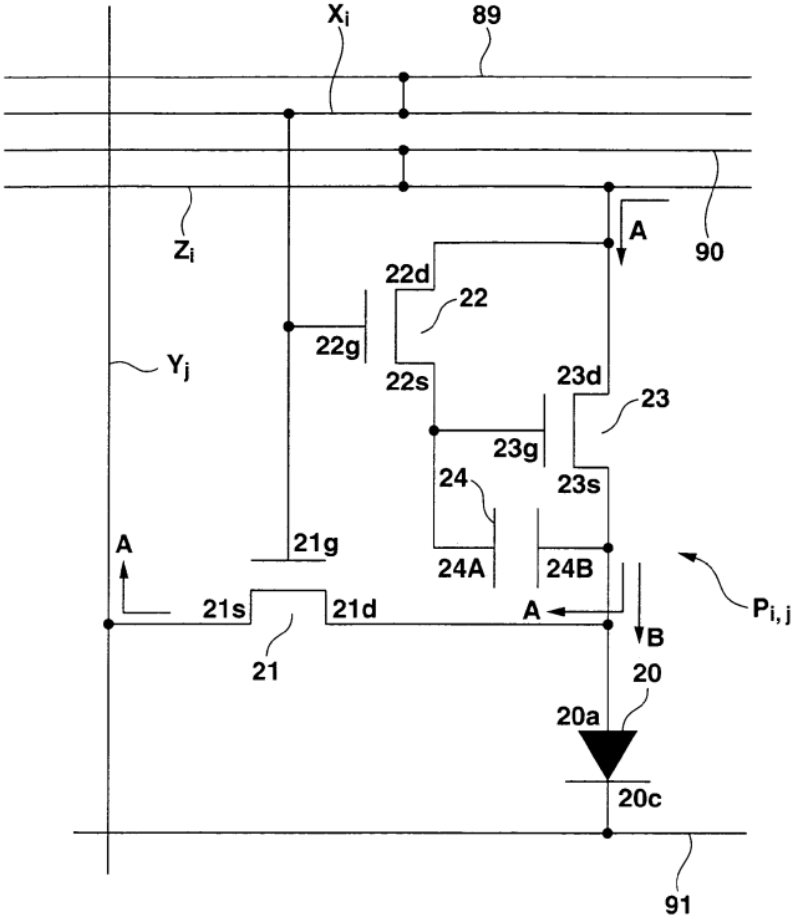


FIG.2

Figure 2 shows the sub-pixel circuit arrangement, which includes organic electroluminescence (EL) element 20, switch transistor 21, holding transistor 22, driving transistor 23, and capacitor 24. *Id.* at 6:48–55. Further, scan line Xi is electrically connected to select interconnection 89, switch transistor 21, and holding transistor 22; signal line Yj is electrically connected to switch transistor 21; and supply line Zi is electrically connected to feed

interconnection 90 and driving transistor 23. *Id.* at 6:61–62, 6:65–67, 7:3–6, 7:11–13, 14:47–50.

The '338 patent describes two operating periods for the pixel circuit: a "selection period" and a subsequent "light emission period." *Id.* at 15:28, 15:58–61. During the selection period, a "feed driver applies a write feed voltage VL to supply a write current to the driving transistors 23 connected to" supply line Zi. *Id.* at 14:46–50; *see id.* at Fig. 7. The "write current (pull-out current) . . . flows from the feed interconnection 90 and supply line Zi through the drain-to-source path of the driving transistor 23 and the drain-to-source path of the switch transistor 21" and to signal line Yj. *Id.* at 15:34–41. Notably, "the switch transistor 21 functions to turn on (selection period) and off (light emission period) of the current between the signal line Yj and the source 23s of the driving transistor 23." *Id.* at 17:26–29. That is, switch transistor 21 controls whether the write current flows through driving transistor 23, depending on whether the switch transistor is respectively turned on or off. *See id.*; *see also id.* at 15:58–61. In the "subsequent light emission period," switch transistor 21 is "turned off." *Id.* at 15:58–61.

Furthermore, the '338 patent describes that such pixel circuit arrangements for a display are formed "by stacking various kinds of layers on [an] insulating substrate." *Id.* at 8:21–22. Figure 6, reproduced below, is a cross-sectional view of a pixel showing such stacked layers.

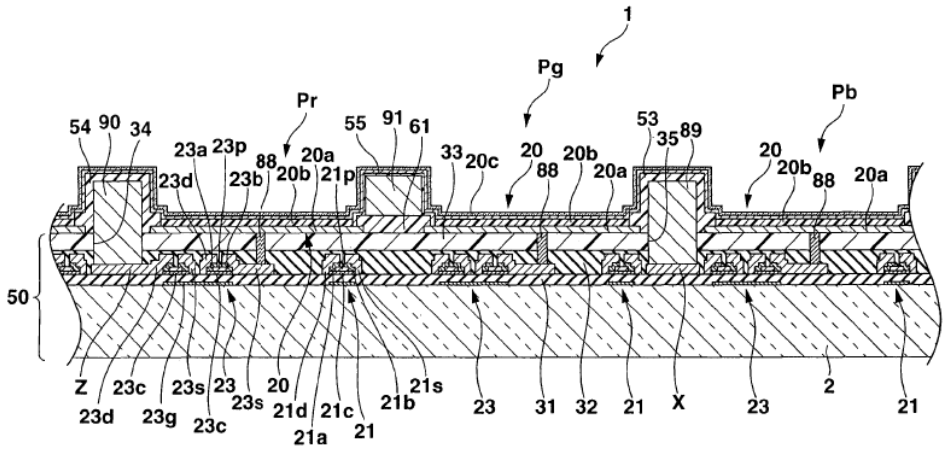


FIG.6

As shown in Figure 6, the aforementioned circuit elements are layered over insulating substrate 2 to form the previously described circuit arrangement. *Id.* at 8:18–53. In particular, transistor array substrate 50 includes transistors 21–23. *Id.* at 8:25–9:2. Interconnections are then stacked to "project upward from the upper surface of the planarization film 33" (*id.* at 11:39–41), i.e., the surface of the transistor array substrate (*id.* at 10:45–47; *see id.* at 10:49–50). Further, "sub-pixel electrodes 20a are arrayed in a matrix on . . . the upper surface of the transistor array substrate 50" (*id.* at 11:50–52) and "organic EL layer 20b of the organic EL element 20," i.e., a light-emitting layer, "is formed on the sub-pixel electrode 20a" (*id.* at 12:14–16). Additionally, "counter electrode 20c functioning as the cathode of the organic EL element 20 is formed on the organic EL layers 20b." *Id.* at 13:28–30.

B. Illustrative claim

Of the challenged claims, claim 1 is independent and is reproduced below.

1. A display panel comprising:

a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain;

a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other;

a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate;

a plurality of light-emitting layers formed on the pixel electrodes, respectively; and

a counter electrode which is stacked on the light-emitting layers,

wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

C. Related Proceedings

Petitioner and Patent Owner identify the following related litigation asserting the '338 patent: *Solas OLED Ltd. v. Samsung Display Co., Ltd., et al.*, Case No. 2:19-cv-00152-JRG (E.D. Tex.); *Solas OLED Ltd. v. Apple Inc.*, Case No. 6:19-cv-00527 (W.D. Tex.); and *Solas OLED Ltd. v. Google Inc.*, Case No. 6:10-cv-00515 (W.D. Tex.). Pet. 9; Paper 3, 1–2.

D. References

Petitioner relies on the following references:

1. "Kobayashi" (US 2002/0158835 A1; published Oct. 31, 2002) (Ex. 1003);

2. "Shirasaki" (US 2004/0113873 A1; published June 17, 2004) (Ex. 1004); and

3. "Childs" (WO 03/079441 A1; published Sept. 25, 2003) (Ex. 1005).[2]

E. Grounds Asserted

Petitioner asserts that claims 1–3 and 5–13 are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §	References/Basis
1, 2, 5, 6, 9–11	103	Kobayashi, Shirasaki
1–3, 5–13	103	Childs, Shirasaki

Petitioner also relies on testimony from Adam Fontecchio, Ph.D. (Ex. 1018, "Fontecchio Decl.").

[2] Patent Owner contends the Examiner considered Childs during prosecution because Childs was disclosed in an Information Disclosure Statement, and the Examiner considered references with three-transistor circuits similar to Shirasaki. Prelim. Resp. 8–13. Patent Owner does not ask us to exercise our discretion to deny institution under 35 U.S.C. § 325(d) or apply the factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (Dec. 15, 2017) (precedential). *See* Prelim. Resp. 8–13. On this record, and particularly in view of the evidence and facts presented in the Petition as discussed below, we do not exercise our discretion under § 325(d).

II. ANALYSIS

A. Legal Principles

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in the record, objective evidence of nonobviousness. *See Graham v. John Deere Co*., 383 U.S. 1, 17–18 (1966). In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418.

B. Level of Ordinary Skill in the Art

Petitioner asserts one of ordinary skill in the art at the time of the invention "would have had a relevant technical degree in electrical engineering, computer engineering, physics, or the like, and 2–3 years of experience in active matrix display design and/or manufacturing." Pet. 21 (citing Ex. 1018 ¶¶ 73–74). Patent Owner does not address the level of ordinary skill in the art. *See generally* Prelim. Resp.

For purposes of this decision, we adopt Petitioner's formulation because it is consistent with the '338 patent and the asserted prior art.

C. Preliminary Matters

In its Supplemental Response Brief, Patent Owner contends that Petitioner improperly makes new arguments in Petitioner's Supplemental Brief that were not present in the Petition. Supp. Resp. Br. 3–5. Patent Owner contends these new arguments are outside the purpose for which we authorized supplemental briefing (i.e., addressing the district court's claim construction order). *Id.* at 4–5. We agree with Patent Owner that, to the extent Petitioner uses its Supplemental Brief to change the theories in its Petition or to reply to the Preliminary Response, we did not authorize supplemental briefing for those purposes. Instead, we authorized supplemental briefing to address the district court's claim construction order. Ex. 3002. To the extent Petitioner makes new arguments in its supplemental brief not in its Petition, we do not consider those arguments in determining whether to institute an *inter partes* review for this proceeding.

D. Claim Construction

In the Petition, Petitioner addresses the construction of three claim terms: "transistor array substrate," "a plurality of interconnections which are formed to project from a surface of the transistor array substrate," and "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." Pet. 21–26. Patent Owner does not directly address Petitioner's proffered claim constructions. *See* Prelim. Resp. 3–8; Supp. Resp. Br. 2–5.

After Patent Owner filed its Preliminary Response, the Eastern District of Texas issued a Claim Construction Memorandum and Order in a related case involving these parties and the '338 patent. Ex. 1020. We authorized the parties to file the district court's claim construction order as

well as supplemental briefing "limited to addressing that district court claim construction order." Ex. 3002.

We have considered the district court's claim construction order (37 C.F.R. § 42.100(b)), as well as the parties' supplemental briefing other than as discussed above. The parties' supplemental briefing is directed to the district court's constructions of "write current" and "transistor array substrate," as recited in claim 1 of the '338 patent *See* Supp. Br.; Supp. Resp. Br.

1. "write current"

The district court construed "write current" to mean "pull-out current" based primarily on intrinsic evidence equating the terms. Ex. 1020, 18–23. Petitioner's supplemental brief states "to the extent that the Board applies the 'pull-out current' construction (which [Petitioner] advanced in the district court subsequent to filing this IPR), the limitation is met by the Shirasaki pixel circuit as advanced in the Petition." Supp. Br. 3. Petitioner, however, does not provide further explanation as to a "pull-out current," or how the construction as "pull-out current" applies to the teachings of the references at issue. *See id.* at 3–5. Patent Owner's Supplemental Response Brief also does not illuminate the proper construction of "write current" or the district court's construction of that term as a "pull-out current," instead focusing on the scope of Petitioner's brief as discussed above. *See* Supp. Resp. Br. 2–5.

Because neither party explains sufficiently the significance of the district court's construction of "write current" as a "pull-out current" to this proceeding, we do not determine at this stage whether it would be appropriate to also adopt that construction here. Instead, we invite the

parties to further address the proper construction of "write current" during the trial.

2. "transistor array substrate"

Petitioner argues that "transistor array substrate" "should be interpreted as covering a layered structure including a bottom insulating substrate through a topmost insulating layer on whose surface the pixel electrodes are formed." Pet. 23 (citing Ex. 1018 ¶ 82); Ex. 1020 (proposing a substantially similar construction in district court). The district court adopted Patent Owner's proposed construction in that proceeding as a "layered structure upon which or within which a transistor array is fabricated." Ex. 1020, 15. Patent Owner has not proposed that construction here, instead arguing only that one of the asserted references (Childs) does not meet Petitioner's proposed construction. *See* Prelim. Resp. 27–28.

In the supplemental briefing, again, neither party argues we should adopt the same construction as the district court. Petitioner argues the limitation is taught by the asserted references under either construction. Supp. Br. 5. Patent Owner emphasizes its Preliminary Response arguments as to this term if we adopt Petitioner's proposed construction, and Patent Owner alternatively relies on its "write current" arguments if we adopt the district court's construction of "transistor array substrate." Supp. Resp. Br. 5.

We find it unnecessary to construe this term at this stage of the proceeding. As with "write current," the proper construction of "transistor array substrate" has not been fully developed by the parties. Thus, we invite the parties to further address the proper construction of this term during the trial.

We determine we need not explicitly construe any claim terms at this stage of the proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

E. Asserted Obviousness over Kobayashi and Shirasaki

1. Overview of Kobayashi (Ex. 1003)

Kobayashi describes "a planar display device such as an organic electroluminescence (EL) display device" which "includes display elements arranged in a matrix and auxiliary wiring elements." Ex. 1003 ¶ 1, code (57). The arrangement of display elements and auxiliary wiring elements is shown below, in Figure 1.

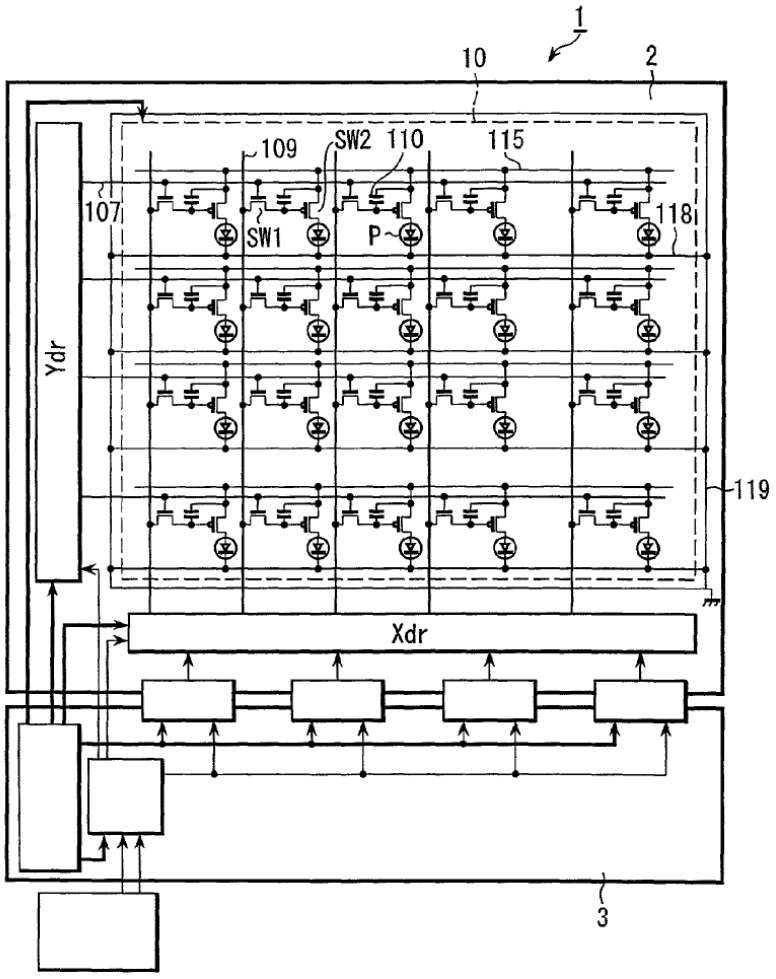
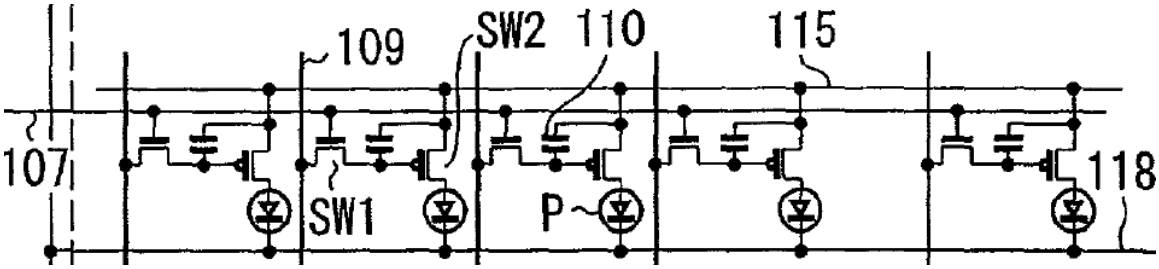


FIG. 1

As shown in Figure 1, organic EL display device 1 has "a display region 10 where the display elements P are arranged in a matrix." *Id.* ¶ 41. There are "three kinds of display elements P, which respectively emit red, green and blue light." *Id.* Further, the display "includes an n-type TFT functioning as a switching element SW1, a capacitor 110 for holding a video signal voltage, [and] a p-type TFT functioning as a driving control element SW2." *Id.* ¶ 43. The display still further includes signal lines, in particular, "scan signal line drive circuit Ydr for supplying drive pulses to the scan

signal lines 107 and a video signal line drive circuit Xdr for supplying drive signals to the video signal lines 109." *Id.* ¶ 42.

The arrangement of the display components is shown below, in an enlarged portion of Figure 1.



As shown in the enlarged portion of Figure 1, "driving control element SW2 is connected in series to the organic EL display element P." *Id.* ¶ 43. In particular, driving control element SW2 connects organic EL display element P to "an organic EL current supply line 115." *See id.* ¶ 70. Further, "video signal voltage holding capacitor 110 is connected in series to the switching element SW1 and in parallel to the driving control element SW2." *Id.* ¶ 43.

Furthermore, Kobayashi's display elements and associated interconnections may be formed in layers on an insulating support substrate, as shown below in Figure 7.

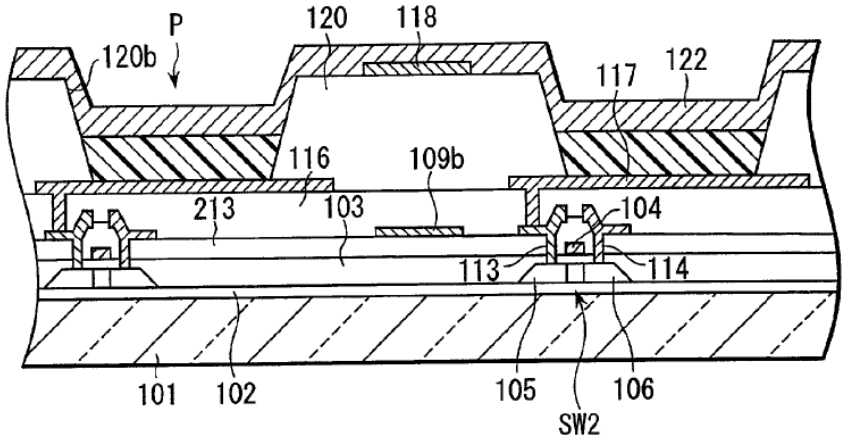


FIG. 7

In particular, Figure 7 shows

> first electrode 117 formed of a light-reflecting conductive film, which is connected to the driving control element SW2; an organic light-emission layer 121 functioning as a light active layer, which is disposed on the first electrode 117; and a second electrode 122 disposed to be opposed to the first electrode 117 via the organic light-emission layer 121.

Id. ¶ 44.

2. Overview of Shirasaki (Ex. 1004)

Shirasaki describes a "circuit configuration of [a] pixel driving circuit" for a display panel. Ex. 1004 ¶¶ 1, 68. Figure 5B, reproduced below, shows a circuit diagram for driving two adjacent pixels during a non-selection period. *Id.* ¶¶ 32, 44.

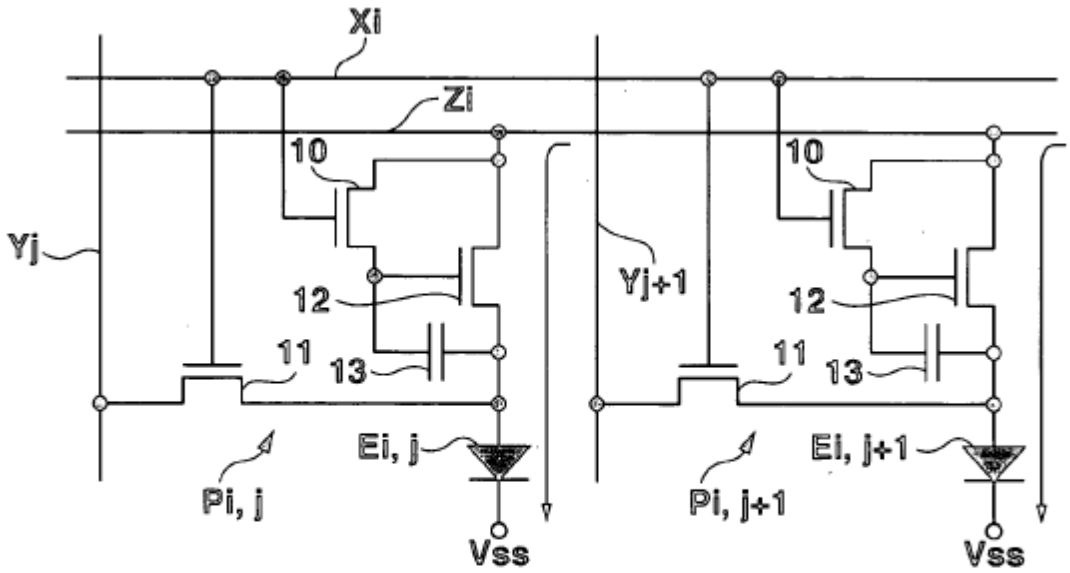


FIG.5B

The pixel driving circuit for pixel Pi, j (the pixel on the left-hand side of Figure 5B) includes three transistors 10, 11, and 12, capacitor 13, and organicEL element Ei, j. *Id.* ¶ 68. During a selection period, transistor 11 is

turned on and a current is supplied "between the source and drain of the transistor 12 through the current line Y, in accordance with the image data." *Id.* ¶¶ 84, 92. Also during the selection period, "transistor 10 is turned on . . . and a voltage is applied to . . . capacitor 13" (*id.* ¶ 84) which "stores electric charge, as current data, which has a magnitude corresponding to the current value" (*id.* ¶¶ 72, 91). During a non-selection period, transistor 11 is turned off and "display current equal to the extracted memory current [is supplied] to the organic EL element E." *Id.* ¶¶ 88, 92. In particular, "transistor 12 can supply a desired electric current corresponding to the image data" to organic EL element Ei, j. *Id.* ¶ 92.

3. Analysis

Petitioner contends claims 1–2, 5–6, and 9–11 are unpatentable as obvious over Kobayashi and Shirasaki. Pet. 38–62. We have reviewed the information provided by Petitioner, including the relevant portions of the supporting Fontecchio Declaration (Ex. 1018), and are persuaded, based on the current record, that Petitioner has demonstrated a reasonable likelihood of prevailing on this obviousness challenge.

Petitioner contends that Kobayashi teaches all of the limitations of claim 1, except that Kobayashi teaches only a two-transistor circuit for each pixel, rather than the three-transistor circuit recited in claim 1. *See* Pet. 39–52. We have reviewed these contentions as well as the cited supporting evidence and find them sufficient at this stage of the proceeding.

For example, claim 1 recites "a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain." Ex. 1001, 24:15–18. Petitioner contends Kobayashi teaches this limitation. Pet. 39–43. In particular, Petitioner argues

Kobayashi's layered structure as depicted in Figure 7 teaches the "transistor array substrate," display elements P are "pixels," and switching element SW1 and driving control element SW2 teach "a plurality of transistors for each pixel." *Id.* (citing Ex. 1003 ¶¶ 41, 43, 60, 64, 66, 68–71, 73, 80, 84, 90–91, Fig. 7; Ex. 1018 ¶¶ 106–114).

Claim 1 further recites "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other." Ex. 1001, 24:19–21. For this limitation, Petitioner contends "Kobayashi discloses 'auxiliary wiring elements 118 [that] are interconnected over the entire display region 10' and that project from the surface of 'insulating layer 116' (i.e., the surface of the claimed transistor array substrate)." Pet. 44–45 (citing Ex. 1003 ¶¶ 62, 83, 88, Fig. 7; Ex. 1018 ¶¶ 115–117). Petitioner further contends Kobayshi's "'auxiliary wiring elements 118' (the claimed plurality of interconnections) are arrayed in parallel to each other: 'auxiliary wiring elements 118 . . . are disposed in a lattice shape.'" *Id.* at 45–46 (quoting Ex. 1003 ¶ 88; citing *id.* at Fig 1; Ex. 1018 ¶ 118).

Claim 1 also recites "a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." Ex. 1001, 24:22–25. Petitioner contends Kobayashi's "first electrodes 117" teach this limitation. *See* Pet. 46–49 (citing Ex. 1003 ¶¶ 44, 46, 51, 57, 71, 74, 90, 92, Fig. 7; Ex. 1018 ¶¶ 120–123).

Claim 1 also recites "a plurality of light-emitting layers formed on the pixel electrodes, respectively." Ex. 1001, 24:26–27. Petitioner contends "Kobayashi discloses 'organic light-emission layers 121' that are 'formed

on'/'disposed on' each 'first electrode 117' in each 'display element P.'" Pet. 49 (citing Ex. 1003 ¶¶ 44, 79–80, 92; Ex. 1018 ¶ 125).

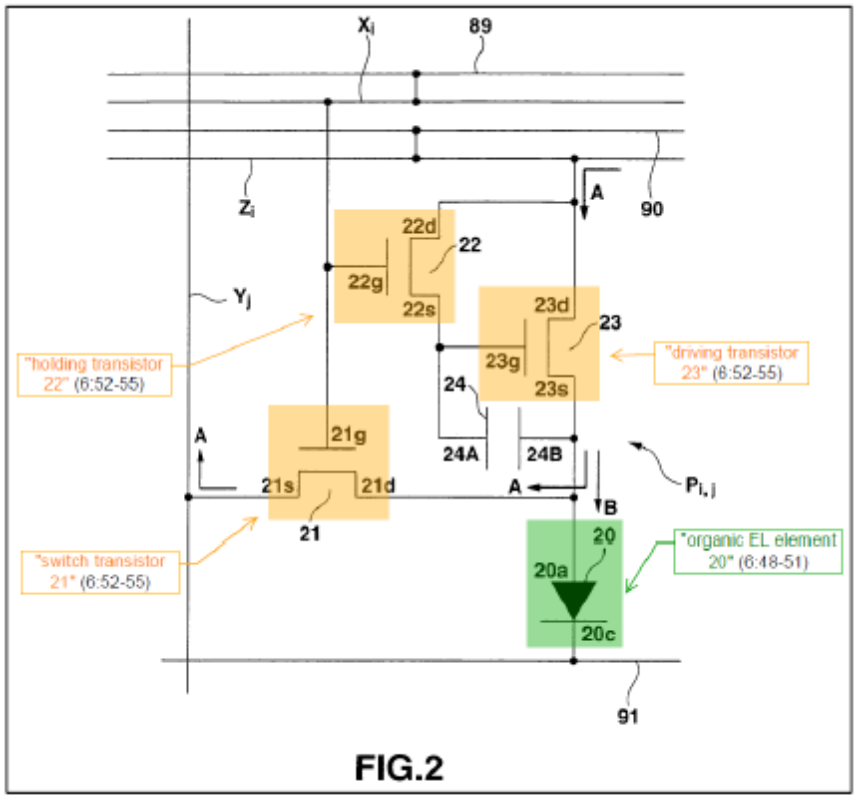
Claim 1 further recites "a counter electrode which is stacked on the light-emitting layers." Ex. 1001, 24:28–29. Petitioner contends "Kobayashi discloses a counter electrode (second electrode 12) which is stacked on the light-emitting layers (organic light-emission layers 121)." Pet. 49–50 (citing Ex. 1003 ¶¶ 44, 51, 57, 80; Ex. 1018 ¶ 127).

Claim 1 also recites:

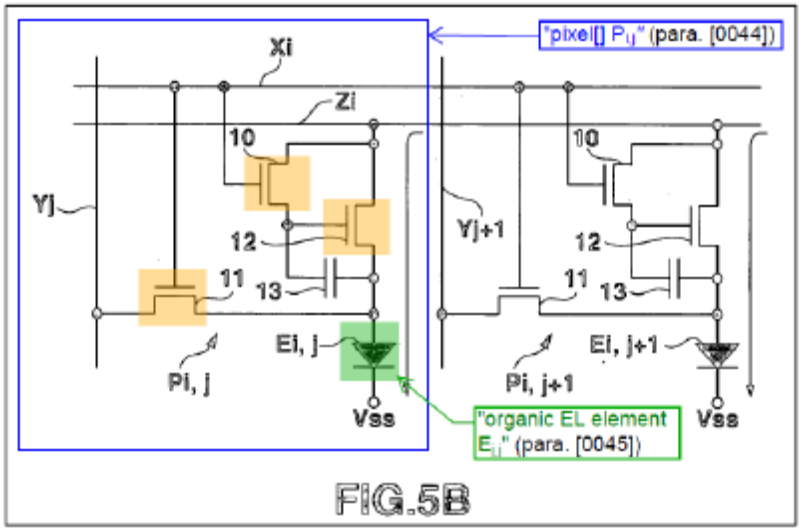
> wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

Ex. 1001, 24:31–38. Petitioner contends the combination of Kobayashi and Shirasaki teaches this limitation. Pet. 50–57. Specifically, Petitioner contends "Kobayashi discloses that each pixel includes the claimed 'driving transistor' and 'switch transistor,' and it would have been obvious to further incorporate the claimed 'holding transistor' in view of Shirasaki." *Id.* at 50.

Petitioner provides an annotated version of Figure 2 of the '338 patent and an annotated version of Figure 5B of Shirasaki, as reproduced below (*id.* at 52–53).



Ex. 1001 ('338 patent), Fig. 2 (annotated).



Ex. 1004 (Shirasaki), Fig. 5B (annotated).

The annotated figures above show the three-transistor pixel circuits in the '338 patent and Shirasaki. As Petitioner notes (*id.* at 52), these circuits are substantially the same.

In explaining the combination of Kobayashi's and Shirasaki's teachings, Petitioner argues Shirasaki discloses "replacing a two-transistor-per-pixel circuit structure (as in Kobayashi) with a three-transistor-per-pixel circuit that includes each of the claimed 'driving transistor,' 'switching transistor,' and 'holding transistor.'" *Id.* at 51; *see also id.* at 56–57 (discussing reasonable expectation of success). Petitioner points to disadvantages of two-transistor circuits discussed in Shirasaki. *Id.* at 53–54 (quoting Ex. 1004 ¶ 7 ("difficult to display images with a desired luminance tone for long time periods"; "no accurate tone control"; "difficult to make the characteristics of the transistors [] of the individual pixels uniform"). Petitioner further argues Shirasaki discloses advantages to replacing a two-transistor circuit with Shirasaki's three-transistor circuit. *Id.* at 54–55 (quoting Ex. 1004 ¶¶ 18 ("Current control is thus performed by the current values, not by voltage values. This suppresses the influence of variations in the voltage-current characteristic of the control system and allows the optical element to stably display images with desired luminance."), 11 ("[O]ne advantage of the present invention is that pixels stably display image with desired luminance in a display panel.")). We find this explanation sufficient at this stage of the proceeding and based on the current record to show that a person of ordinary skill in the art would have found it obvious to replace Kobayashi's two-transistor pixel circuit with the three-transistor circuit of Shirasaki.

As to this challenge, Patent Owner focuses its arguments on the "write current" recited in claim 1 ("a switch transistor which makes a *write current* flow between the drain and the source of the driving transistor"), and in particular, Patent Owner argues Petitioner relies only on Kobayashi for this limitation without adequately explaining how Kobayashi teaches a "write

current." Prelim. Resp. 1–2, 8, 13–22. We agree with Patent Owner that Petitioner discusses the "write current" in the context of Kobayashi. Pet. 50–51 (arguing that "switching elements SW1" in Kobayashi correspond to the claimed "switching transistor which makes a write current flow between the drain and the source of the driving transistor" and that SW1 controls "whether a current flows between the drain and source of driving transistor SW2"). Nevertheless, we find as discussed above that Petitioner explains the combination as replacing Kobayashi's two-transistor circuit with Shirasaki's three-transistor circuit. Thus, we are not persuaded presently by Patent Owner's arguments addressing Kobayashi's "write current" because those arguments address Kobayashi individually, rather than the combination of teachings on which Petitioner relies. *See In re Keller*, 642 F.2d 413, 426 (CCPA 1981) (citation omitted) ("[O]ne cannot show non-obviousness by attacking references individually where . . . the rejections are based on combinations of references.").

We also agree with Patent Owner (*see* Prelim. Resp. 20–22) that Petitioner does not specifically identify the "write current" in replacing Kobayashi's two-transistor circuit with Shirasaki's three-transistor circuit. Nevertheless, we find it sufficiently clear from the Petition that Petitioner maps transistor 11 in Shirasaki Figure 5B to the recited "switching transistor." *See* Pet. 52–53. Patent Owner also appears to understand Petitioner's contentions this way. Prelim. Resp. 21–22. Because the circuit in Figure 5B of Kobayashi is substantially identical to the circuit disclosed in Figure 2 of the '338 patent, on the current record, it appears that the current flow between the components is also the same (at least in terms of directionality when the corresponding transistors are in the same position). Thus, while Petitioner could have avoided any ambiguity by explicitly

explaining how Shirasaki's transistor 11 makes a write current flow between the drain and the source of transistor 12 (i.e., the driving transistor), we find that explanation unnecessary based on the current record at this stage of the proceeding.

Accordingly, we find that at this stage of the proceeding and based on the current record, that Petitioner has adequately shown that "a switch transistor which makes a write current flow between the drain and the source of the driving transistor" would have been obvious based on the combination of Kobayashi's and Shirasaki's teachings. We find Petitioner's contentions, detailed above and supported by the Fontecchio Declaration, are sufficient to show a reasonable likelihood of success for this challenge to claim 1.

Petitioner also provides further analysis detailing where it contends each additional limitation of claims 2, 5, 6, and 9–11 are taught in Kobayashi, which we find sufficiently persuasive on the current record and at this stage of the proceeding. Pet. 58–62.

We determine Petitioner has shown a reasonable likelihood of prevailing with respect to its challenge to claims 1, 2, 5, 6, and 9–11 as unpatentable as obvious over Kobayashi and Shirasaki.

F. Asserted Obviousness over Childs and Shirasaki

1. Childs (Ex. 1005)

Childs describes an active-matrix electroluminescent display (AMELD) having an array of pixels on a circuit substrate. Ex. 1005, 6:23–25. Figure 1, reproduced below, shows an array of four pixels, the pixels having an exemplary pixel circuit configuration. *Id.* at 5:3–5.

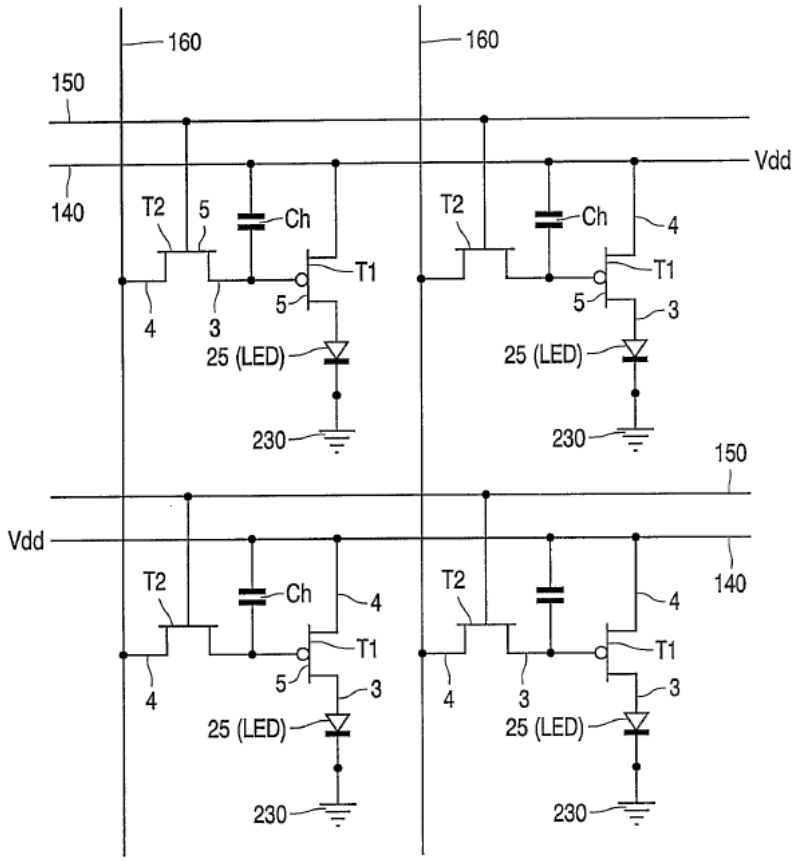


FIG. 1

As shown in Figure 1, for each respective pixel circuit, "pixel 200 comprises a current-driven electroluminescent display element 25," e.g., light-emitting diode (LED) of organic semiconductor material; two transistors, i.e., drive element T1 and addressing element T2; and a holding capacitor Ch. *Id.* at 7:3–6, 10–14, 25. In the pixel circuit, "LED 25 is connected in series with a drive element T1 (typically a [thin-film transistor (TFT)]) between two voltage supply lines 140 and 230" such that "[l]ight emission from the LED 25 is controlled by the current flow through the LED 25, as altered by its respective drive TFT T1." *Id.* at 7:12–17.

Furthermore, "[e]ach row of pixels is addressed in turn in a frame period by means of a selection signal" which "turns on the addressing TFT

T2, [and] so loading the pixels of that row with respective data signals from the column conductors 160." *Id.* at 7:18–22. The "data signal is maintained on [TFT T2's] gate 5 by a holding capacitor Ch." *Id.* at 7:24–25. Accordingly, "the drive current through the LED 25 of each pixel 200 is controlled by the driving TFT T1 based on a drive signal applied during the preceding address period and stored as a voltage on the associated capacitor Ch." *Id.* at 7:26–29.

The aforementioned pixel circuitry is constructed over an insulating layer. *Id.* at 7:31–8:2. The layering of pixel circuitry elements is shown in Figure 2, reproduced below.

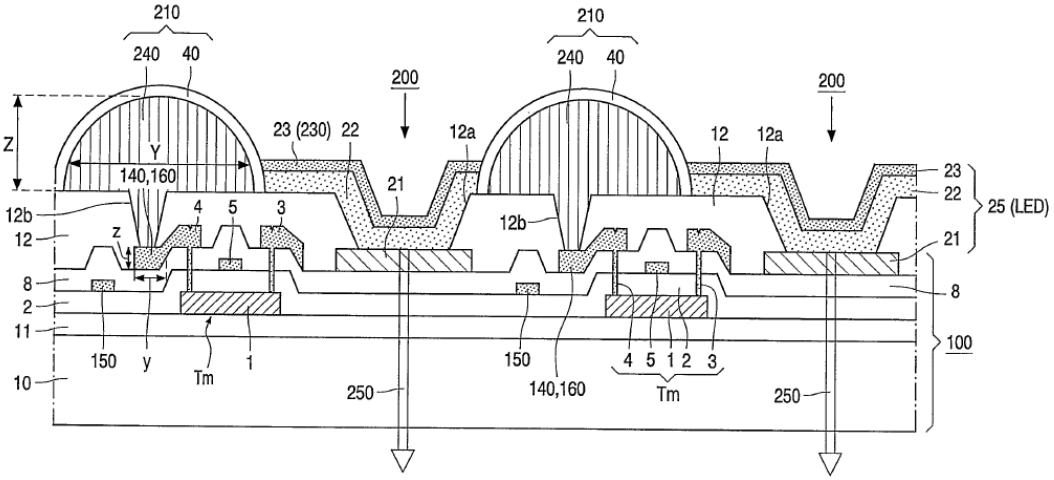


FIG. 2

As shown in Figure 2, TFTs Tm and Tg are layered over insulating glass base 10 and surface-buffer layer 11. *See id.* at 7:32–8:8. Layered over electrodes 3, 4 of the TFTs are "conductor lines 140, 150 and 160," as described above. *Id.* at 8:8–13. And still further layered over TFTs Tm and Tg is LED 25, which "comprises a light-emitting organic semiconductor material 22 between a lower electrode 21 and an upper electrode 23." *Id.* at 8:16–17.

2. Analysis

Petitioner contends claims 1–3 and 5–13 are unpatentable as obvious over Childs and Shirasaki. Pet. 63. We have reviewed the information provided by Petitioner, including the relevant portions of the supporting Fontecchio Declaration (Ex. 1018), and are persuaded, based on the current record, that Petitioner has demonstrated a reasonable likelihood of prevailing on this obviousness challenge.

Petitioner contends that Childs teaches all of the limitations of claim 1, except that Kobayashi teaches only a two-transistor circuit for each pixel, rather than the three-transistor circuit recited in claim 1. *See* Pet. 64–82. We have reviewed these contentions as well as the cited supporting evidence and find them sufficient at this stage of the proceeding.

For example, claim 1 recites "a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain." Ex. 1001, 24:15–18. Petitioner contends Childs teaches this limitation. Pet. 64–68 (citing Ex. 1005, 6:23–27, 7:10–8:27, 10:25–27, 14:30–32, Fig. 2; Ex. 1018 ¶¶ 165–170). In particular, Petitioner contends "Childs describes the layered structure of 'circuit substrate 100,' which extends from 'insulating glass base 10' through 'insulating layers' 11, 2 and 8 and 'planar insulating layer 12.'" *Id.* at 64 (citing Ex. 1005, 6:23–25, 7:31–8:27, 14:30–32). Petitioner provides an annotated version of Figure 2 of Childs and also relies on the testimony of Dr. Fontecchio in support. *Id.* at 64–65 (citing Ex. 1005, Fig. 2; Ex. 1018 ¶¶ 165–66).

Under the construction adopted by the district court (and proposed by Patent Owner there, namely, a "layered structure upon which or within which a transistor array is fabricated"), Patent Owner does not appear to

dispute that Childs teaches the recited "transistor array substrate." Supp. Resp. Br. 5; Ex. 1020, 8–15. Patent Owner, however, argues Childs does not teach a "transistor array substrate" under the construction proposed by Petitioner here and in the district court (namely, a "layered structure including a bottom insulating substrate through a topmost insulating layer on whose surface the pixel electrodes are formed," Pet. 23; Ex. 1020, 8). Prelim. Resp. 27–28. Pointing to Figure 2 of Childs as annotated by Petitioner, Patent Owner argues layer 12 cannot be part of the transistor array substrate because the layer 8 would be the "topmost insulating layer on whose surface the pixel electrodes are formed," under Petitioner's proposed construction. *Id.* (citing Pet. 69).

Patent Owner, however, does not address Petitioner's contentions in the context of the limitation, "the pixel electrodes being arrayed . . . on the surface of the transistor array substrate." Pet. 71–75. There, Petitioner explains why it would have been obvious to form Child's lower electrode 21 on the surface of the topmost insulating layer, and also relies on the testimony of Dr. Fontecchio in support. *Id.* (citing Ex. 1018 ¶¶ 179–191). We find this explanation sufficiently persuasive at this stage of the proceeding.[3]

Claim 1 further recites "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other." Ex. 1001, 24:19–21. Petitioner

[3] At this stage of the proceeding, we need not and do not determine whether these contentions are necessary or whether Petitioner's alternative argument alone is sufficient (i.e., that layer 8 in Childs is, in fact, the topmost insulating layer because lower electrodes 21 are exposed in connection windows 12a). *See* Pet. 71 (citing Ex. 1005, 8:3–27, Fig. 2; Ex. 1018 ¶ 178).

contends "Childs discloses that its 'physical barriers 210' 'are constructed with conductive barrier material 240 that is used as an interconnection,'" and "conductive barriers 240 are 'deposited on the insulating layer 12,' project from the surface of insulating layer 12 (i.e., from the claimed 'surface of the transistor array substrate'), and are arrayed in parallel to each other." Pet. 68–69 (citing Ex. 1005, 6:25–29, 9:3–11, 9:20–29, 15:9–23, Fig. 2; Ex. 1018 ¶¶ 172–173).

Claim 1 also recites "a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." Ex. 1001, 24:22–25. Petitioner contends Childs teaches this limitation. Pet. 69–75 (citing Ex. 1005, 7:10–12, 8:3–27, 14:29–5:2, Fig. 2; Ex. 1014 ¶¶ 310–311, Fig. 14; Ex. 1017 ¶ 77, Fig. 5b; Ex. 1018 ¶¶ 176–180, 184, 188–191). In particular, Petitioner contends Childs teaches lower electrodes 21 for each pixel, which are arrayed along and between conductive barriers 240 (i.e., "the interconnections") and formed on insulating layer 8 and exposed in connection windows 12a. *Id.* at 71. Additionally, as discussed above in the context of the "transistor substrate array," Petitioner provides an alternative explanation that this limitation would have been obvious even if Childs' insulating layer 8 is not the surface of the transistor array substrate. *See* Pet. 71–75

Claim 1 further recites "a plurality of light-emitting layers formed on the pixel electrodes, respectively." Ex. 1001, 24:26–27. Petitioner contends "Childs discloses that '[e]ach pixel 200 comprises a current-driven electroluminescent display element 25 (21, 22, 23),' and that 'a light-emitting organic semiconductor material 22' is formed 'between' each

'lower electrode 21 and an upper electrode 23.'" Pet. 75–76 (citing Ex. 1005, 7:10–12, 8:16–27, 9:3–11, 15:29–31; Ex. 1018 ¶¶ 194–195).

Claim 1 also recites "a counter electrode which is stacked on the light-emitting layers." Ex. 1001, 24:28–29. Petitioner contends Childs teaches this limitation. Pet. 76 (citing Ex. 1005, 7:10–12, 8:16–27, 8:19–22; Ex. 1018 ¶ 197).

Claim 1 also recites

> wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

Ex. 1001, 24:30–38. Petitioner contends the combination of Childs and Shirasaki teaches this limitation. Pet. 76–82 (citing Ex. 1004, ¶¶ 3–8, 13–19, 41, 43; Fig. 5B; Ex. 1005, 1:5–7, 7:6–30, Fig. 1; Ex. 1018 ¶¶ 201–214). Specifically, Petitioner contends "Childs discloses that the plurality of transistors for each pixel include the claimed 'driving transistor' and 'switch transistor,' and it would have been obvious to further incorporate the claimed 'holding transistor' in view of Shirasaki." *Id.* at 76.

Again, Petitioner provides an annotated version of Figure 2 of the '338 patent and an annotated version of Figure 5B of Shirasaki (*id.* at 78–79), as Petitioner did for the Kobayashi-Shirasaki challenge. As discussed above, those annotated figures show the three-transistor pixel circuits in the '338 patent and Shirasaki are substantially the same.

In explaining the combination of Childs' and Shirasaki's teachings, Petitioner argues a person of ordinary skill in the art would have replaced Childs' two-transistor pixel circuit with Skirasaki's three-transistor pixel

circuit. *Id.* at 79; *see also id.* at 80–81 (discussing reasonable expectation of success). Petitioner points to disadvantages of two-transistor circuits discussed in Shirasaki. *Id.* at 79 (quoting Ex. 1004 ¶ 7 ("difficult to display images with a desired luminance tone for long time periods"; "no accurate tone control"; "difficult to make the characteristics of the transistors [] of the individual pixels uniform"). Petitioner further argues Shirasaki discloses advantages to replacing a two-transistor circuit with Shirasaki's three-transistor circuit. *Id.* at 79–80 (quoting Ex. 1004 ¶¶ 18 ("Current control is thus performed by the current values, not by voltage values. This suppresses the influence of variations in the voltage-current characteristic of the control system and allows the optical element to stably display images with desired luminance."), 11 ("[O]ne advantage of the present invention is that pixels stably display image with desired luminance in a display panel.")). We find this explanation sufficient at this stage of the proceeding and based on the current record to show that a person of ordinary skill in the art would have found it obvious to replace Childs' two-transistor pixel circuit with the three-transistor circuit of Shirasaki.

Patent Owner argues Petitioner relies only on Childs for this limitation without adequately explaining how Childs teaches a "write current." Prelim. Resp. 3, 8, 23–27. We agree with Patent Owner that Petitioner discusses the "write current" in the context of Childs. Pet. 76–77. Nevertheless, we find Petitioner explains the combination as replacing Childs' two-transistor circuit with Shirasaki's three-transistor circuit. *Id.* at 79–82. Thus, we are not persuaded presently by Patent Owner's arguments addressing Childs' "write current" because those arguments address Childs individually, rather than the combination of teachings on which Petitioner relies. *See Keller*, 642 F.2d at 426 (CCPA 1981) (citation omitted).

We also find it sufficiently clear from the Petition that Petitioner maps transistor 11 in Shirasaki Figure 5B to the recited "switching transistor." *See* Pet. 78–79. Because the circuit in Figure 5B of Shirasaki is substantially identical to the circuit disclosed in Figure 2 of the '338 patent, on the current record, it appears that the current flow between the components is also the same (at least in terms of directionality when the corresponding transistors are in the same position). Thus, while Petitioner could have avoided any ambiguity by explicitly explaining how Shirasaki's transistor 11 makes a write current flow between the drain and the source of transistor 12 (i.e., the driving transistor), we find that explanation unnecessary based on the current record at this stage of the proceeding.

Accordingly, we find that at this stage of the proceeding and based on the current record, Petitioner has adequately shown that "a switch transistor which makes a write current flow between the drain and the source of the driving transistor" would have been obvious based on the combination of Childs' and Shirasaki's teachings. We find Petitioner's contentions, detailed above and supported by the Fontecchio Declaration, are sufficient to show a reasonable likelihood of success for this challenge to claim 1.

Petitioner also provides further analysis detailing where it contends each additional limitation of claims 2, 3, and 5–13 are taught in Childs, which we find sufficiently persuasive. Pet. 82–92.

We determine Petitioner has shown a reasonable likelihood of prevailing with respect its challenge to claims 1–3 and 5–13 as unpatentable as obvious over Childs and Shirasaki.

III. CONCLUSION

We determine that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenges to claims 1–3 and 5–13 of the '338 patent as set forth above. At this stage of the proceeding, we have not made a final determination as to the patentability of any of these challenged claims or the construction of any claim term.

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–3 and 5–13 of the '338 patent on the grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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